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Porous silicon as a stationary phase for shear-driven chromatography

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Abstract

We report on the possibility to strongly increase the mass loadability and retention capacity of shear-driven chromatography (SDC) channels by growing a thin porous silicon layer on the stationary wall part. The thickness of the produced porous silicon layers was found to increase linearly with the anodisation time, and could easily be varied between 50 and 300 nm. Combining these layers with sub-μm thin flow-through channels, we believe it is the first time a sub-μm on-chip LC system with a phase ratio similar to that in packed column HPLC (i.e., $V_s/V_m \cong 1.5$) is obtained. The chromatographic performance of the produced channels has been tested by separating binary mixtures of coumarin dyes under RP-LC conditions. The plate height measurements, yielding $H_{min} \cong 0.5\,\mu m$ (corresponding to more than 2×10^6 plates/m) for a retained component with $k'' = 3$, showed good agreement with the theoretical expectations. Due to the presence of some macroscopic defects in the prepared layers, the quality of the separations could however only be maintained over a few millimeters of the channel length. This length was however more than sufficient to separate the coumarin mixture, given the extremely small plate heights of the system.

Keywords: Shear-driven chromatography; Chip technology; Instrumentation; Stationary phases, LC

1. Introduction

The poor mass loadability, and the correspondingly large detection limits are generally considered as the Achilles' heel of analytical laboratory-on-a-chip devices [1,2]. This holds especially for shear-driven chromatography (SDC), a recently introduced alternative [3–5] for the customary used pressure- and electrically-driven chromatographic separation methods, and allowing to achieve large gains in separation resolution and speed, provided the technique is carried out in flat-rectangular channels with a thickness of the order of 0.1–2 μm. The SDC principle is based on the use of channels which are divided into two, non-sealed and independently moving parts. By axially sliding one part of the channel past the other, the viscous drag effect establishes a net flow with a linear velocity gradient.

In a number of previous studies [4–6], we have demonstrated that the enhanced mass transfer kinetics in the SDC nano-channel chip devices can be exploited to yield extremely short separation times. This gain stems from the fact that in a shear-driven channel the mobile phase flow is generated without the aid of an electrical field or an external pump, hence allowing to circumvent the pressure- and the voltage-drop limitation on the mobile phase velocity in pressure- and electrically-driven on-chip separation systems. Using 200 nm thin channels etched into fused-silica optical flats and coated with a monolayer C_{18} stationary phase, a mixture of two coumarin dyes could be separated in less than 0.1 s, without really pushing the system to its limits [5]. As they were only coated with a monolayer C_{18} stationary phase, the retentive power and the mass loadability of the mono-layer coated system was however very low. The lack of retention capacity is a problem which is in fact common to all open-tubular chromatography systems, both electrically- and pressure-driven, and has been the subject of many research efforts in the past [7–10].

To drastically enlarge the retention surface and the mass loadability of the channels needed for SDC, the present study explores the use of a porous silicon stationary phase. Theoretical calculations have namely pointed out that in open-tubular LC one could easily afford to use stationary phases with a thickness of the same order as the diameter of the channel [11]. In [6], we have shown for open-tubular SDC that, when for example using a 200 nm porous stationary phase layer in combination with a 200 nm channel (i.e., working at a phase ratio of $V_s/V_m = 1$), the analysis time would only increase with a factor 2 (leaving the analysis time

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still in the sub-second range for most separations), while the mass loadability, and hence the detection sensitivity, can be increased a 10–100-fold.

Whereas for electrically-driven flow systems the use of silicon-based layer deposition technique is prohibited because of the poor electrical isolation of silicon substrates, shear-driven flows do not raise this problem, such that the relatively simple and well-established methods [12–14] for the generation of thin porous silicon layers can be applied for the generation of a nanometric thin porous layer with a uniform pore structure. Porous silicon is a semiconductor material with a large specific surface area (hundreds of m^2/cm^3) and is produced through electrochemical anodization or chemical etching of crystalline silicon [12,13,15]. The thickness of the layers can be very precisely controlled by the anodisation time and can typically be varied between a few tens of nanometers to about 100 μm [16]. Porous silicon has already found applications in diverse fields such as the development of solar cells [17], micro optics [18], (bio)chemical sensor technology [19] and micro reactors for enzymatic digestion [20]. In the field of analytical chemistry, porous silicon has recently also been introduced [15,21] as a powerful alternative to the traditional matrices for matrix-assisted laser desorption ionization (MALDI) MS analysis (cf. the so-called DIOS-process). With its relatively large specific surface area (typically 180–230 m^2/cm^3 [22]) and its pore sizes in the range of 2–15 nm [23], porous silicon is however also ideally suited as a chromatographic stationary phase layer. In this respect, the very large porosities (up to 80–90%) which can be achieved should also be considered as an interesting advantage. This feature can be exploited to obtain large stationary phase mass transfer rates, although the use of large porosities of course compromises the available specific surface area. Another advantage is that, by simply oxidizing the obtained structures in ambient air, the internal pore surface of the layers can namely very easily be covered with an atomically thin layer of silicon dioxide. This should allow to use the same derivatization procedures as for porous silica [24].

2. Experimental

2.1. Channel lay-out and experimental set-up

A schematic view of the employed experimental set-up is shown in Fig. 2. The central part of the set-up is the SDC channel, formed by two separate channel plates: a small, rectangular silicon plate (dimensions 20 mm × 15 mm) carrying a bundle of several parallel half-open channels (as shown on the surface of the rectangular plate in Fig. 1a) with a porous silicon layer arranged on their bottom, and a larger, round fused-silica wafer (diameter = 5 cm, thickness 1 cm and flatness λ/10, with λ = 512 nm). Whereas the former is used as the stationary channel wall, the latter serves as the moving wall of the SDC channel. After assembly (cf. Fig. 1b), the SDC channel is positioned exactly above the objective lens (Achroplan 4×/0.1, Zeiss, Belgium) of an inverted fluorescence microscope (Axiovert 200, Zeiss, Belgium). For this purpose, the fused-silica wafer is fitted into a stainless steel holder mounted on top of the translation stage of the microscope. The stationary wall part of the channel system is held in place using a second holding frame, precisely fitting around the rectangular silicon plates, and kept stationary by attaching it to the main housing of the microscope, which in turn is mounted on a breadboard (M-IG 23-2, Newport, The Netherlands). The displacement of the fused-silica wafer during the injection procedure (see Section 2.3) and the subsequent separation runs was effectuated using a linear displacement stage (M-531.5 I Intellistage, ALT, Belgium) equipped with a five-phase stepping motor (20,000 steps/revolution) and an integrated motion controller, offering a positioning accuracy of 0.1 μm and a maximal displacement velocity of 8 mm/s. The translation stage was mounted on the same breadboard as the microscope, and was directly connected to the translation table of the microscope using another laboratory made connection piece. In the present study, the translation velocity was varied between 1 and 8 mm/s, corresponding to a mobile zone velocity range lying between 0.5 and 4 mm/s. During the

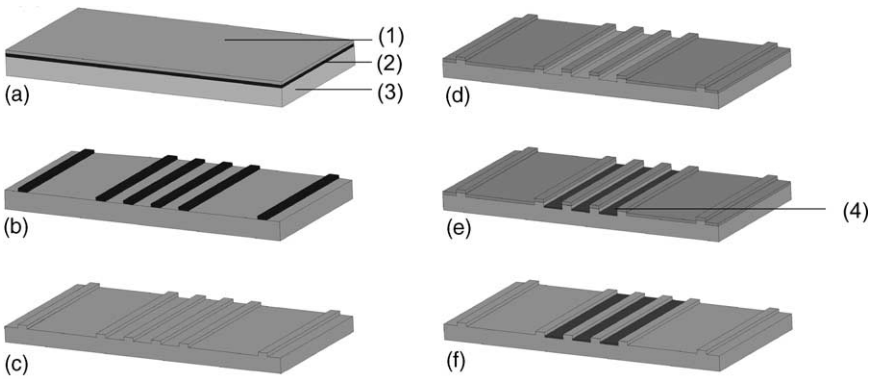

Fig. 1. Different steps in the manufacturing procedure followed to obtain stationary channel wall plates carrying three parallel nano-SDC channels with a thin layer of porous silicon on their bottom surface. The different steps (a–f) and the material of the different layers (1–4) are described in the text (Section 2.2).

operation, a relatively large pressure was applied on the silicon plate using a pneumatically operated metallic cover lid, exerting a downward force on the stationary channel wall. This force was needed to completely flatten out the silicon plate (thickness = 1 mm), which, due to its natural material stress, displays a natural bend when left freestanding. Typically a 1–2 bar pressure force was needed to sufficiently flatten out the silicon plates. This poses no specific problems, as it was observed that the system could be operated pressures up to 5 bar without any notable increase of the sliding resistance.

2.2. Preparation of the stationary channel wall plates carrying a porous silicon layer

In the first step of the stationary channel wall preparation, 100 to 500 nm deep and 750 μm wide parallel channels were etched on the surface of a double-side polished and 1 mm thick Si wafers [2 in. diameter (1 in. = 2.54 cm), p-type, ⟨1 0 0⟩, boron doped (0.01–0.18 Ω, Compart Technology, UK], using a patterned SiO_2 layer as a resist mask. For this purpose, first a SiO_2 layer was grown on the surface of the Si wafer in a thermal oxidation oven (PEO 601, ATV Technology, Germany). Subsequently, and as shown in Fig. 1a, a thin layer of photoresist was applied with a conventional spin-coater (EC 101, Headway Research, Germany). Via a mask aligner (Karl Suss type MJB 3, Süss MicroTec, Germany), this photoresist layer was subsequently selectively illuminated and removed by developing it with an alkalic solution. The thus selectively bared SiO_2 layer was then selectively etched away using a mixture of 11 ml HF, 110 ml NH_4F and 363 ml water. The remaining SiO_2 pattern (Fig. 1b) is then used as an etching mask for the etching of the bared Si wafer portions. This etching step is effectuated using a 0.8 M KOH at 80 °C, a solution which attacks the Si layer much more aggressively than the SiO_2 layers. Several etching KOH-etching times were considered, yielding channel depths between 100 and 500 nm in a simple linear relation to the employed etching time (etching during 30 s for example yielded a 500 nm deep channel). The remaining SiO_2 strips are then removed using the above mentioned HF solution. The thus bared non-etched portions of the Si wafer serve as the channel spacers in the finally assembled channels (Fig. 2). The mobile zone depth (d) of the thus obtained channels is simply equal to the height of the spacers.

In the second phase of the manufacturing process, the bottom of the nanometric deep channels (Fig. 1c) needs to be anodised to form the desired thin porous silicon layer. Prior to this step, a 500 nm thick layer of aluminum was evaporated on the back side of the Si wafer. After this step, the front side of the wafer was again coated with a thin photoresist layer, which was then again selectively patterned using the same mask as used in the first step. In this way, only the Si spacers produced in the first step are coated with the photoresist (Fig. 1d) and are hence protected during the anodisation process. The actual anodisation step was carried

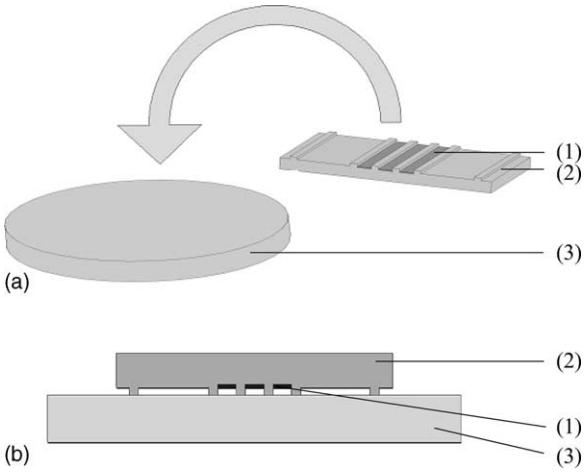

Fig. 2. Schematic drawing (not to scale) of the employed SDC channel system, consisting of a movable, ultra-flat fused-silica plate (3) and the (smaller) silicon plate (2) carrying the porous silicon retentive layer (1). (a) Prior to the assembly (bird's-eye view) and (b) after assembly (cross-sectional view). The image shows how the Si-etched channel spacers allow to maintain a fixed distance between the stationary and moving channel walls.

out using a 5% (v/v) HF solution in a back side contact anodisation cell described elsewhere [14] and equipped with a potentiostat (366A, EG&G) and a Ag/AgCl HF-resistant reference electrode (900600, Thermo Orion). The actual anodisation step was carried out at 0 V Ag/AgCl during 1–15 min (0.3 mA/cm^2). After this step (Fig. 1e), the wafers were successively flushed with pure water, acetone and again water to remove the photoresist from the Si channel spacers (Fig. 1f). Subsequently, the wafers were sawn into 10 mm × 20 mm pieces using a Disco DAD 321 Dicing Saw.

In the third and final step, the porous silicon layers on the stationary channel plates were derivatized by putting them into a 30% (w/w) solution of dimethyloctylchlorosilane (CAS No. 18162-84-0, Sigma–Aldrich, Belgium) in toluene for 48 h at room temperature. During the treatment, the silicon plates were put in a PTFE holder and the coating solution was stirred to maximize the large-scale homogeneity of the coating. Afterwards, the silicon plates were sequentially washed with toluene, methanol, and water.

The quality of the produced layers (mean thickness, uniformity, ...) was tested using scanning electron microscope (SEM; LEO 1550 instrument, LEO Elektronenmikroskopie, Germany).

2.3. Chromatographic procedure and sample and mobile phase composition

All experiments were performed at ambient temperature ($T \cong 20$ °C). The test samples used for the chromatographic separation were prepared by mixing and dissolving two different coumarin dyes (coumarin C440, CAS No. 26093-31-2; and coumarin C450, CAS No. 26078-21-1, Across Organics, Geel, Belgium) at 2.5×10^{-3} mol/l in methanol. For the mobile phase, a wide range of

methanol-water mixtures has been explored by mixing HPLC-grade methanol (v/v) in purified water (Nanopure II, Barnstead, Van Der Heyden, Belgium) at different volumetric ratios. Narrow sample plugs (order 100 μm) were injected in the SDC channels using a dedicated multi-step injection procedure already described previously [5,25]. All presented separation experiments were conducted with the same channel plate, with a depth of 140 nm and a layer thickness of 200 nm.

Prior to each measurement session (typically including some five consecutive runs), the surface was cleaned and dust particles occasionally present on the surfaces of the fused-silica wafer and the silicon plate were washed away with fresh mobile phase liquid. Sometimes, when the first experiment fails (when there is tracer on the channel spacers) extra cleaning with optical quality (C54-601, Scott Pure, Edmund Optics) cleaning tissues was necessary. It would be preferable to work in a clean room but this is not a necessity.

The separations were monitored through the objective lens of the inverted microscope (see Section 2.1), using a Hg-vapor lamp (HBO 103/W2, Zeiss) in combination with a UV filter cube set (F11000, AF Analysentechnik, Germany) to excite the coumarin dyes. The original long-pass emission filter was replaced by a narrow bandpass filter (F3200 D460/50, AF Analysentechnik). The microscope images were recorded using an air-cooled charge coupled device (CCD) fluorescence camera (ORCA-ERG C4742-95-12, Hamamatsu Photonics, Belgium) mounted on the video adapter of the microscope. The camera could be operated at a frame rate of 43 Hz when operated in the 8×8 binding-mode. The video frames were digitally captured using a firewire interface. Subsequent analysis of the video images occurred with the accompanying Simple-PCI 5.1 software.

To characterize the conducted separations in terms of retention factors and theoretical plate heights, a procedure already described previously [5] has been applied. Briefly, the zone retention factor k'' of the sample components was determined from the difference between the position L_0 of the mobile zone (known to move with exactly one half of the moving wall velocity [4]), and the actual position L_{eff} of the moving dye peak, using:

$$k'' = \frac{L_0 - L_{\text{eff}}}{L_{\text{eff}}} \tag{1}$$

The determination of L_0 and L_{eff} can also be assessed from the CCD images. From the variance σ_x^2 of the peaks in the intensity plots, theoretical plate height values were calculated using:

$$H_{\text{exp}} = \frac{\sigma_x^2 - \sigma_{x,\text{inj}}^2}{L_{\text{eff}}} \tag{2}$$

The variance σ_x^2 of the peaks was estimated from the width w_{p} of the peaks in the intensity plots, using $w_{\text{p}} = 4\sigma_x$. The variance of the injected peaks was calculated from the initial width w_{inj} (=110 μm in all presented experiments).

3. Results and discussion

The thickness of the produced porous silicon layers is quite uniform and can very easily be estimated from high resolution SEM pictures. Repeating the anodisation process for a number of different anodisation times, a nearly perfectly linear relation between the layer thickness and the anodisation time was observed. This is in full agreement with the observations presented in [26]. Anodisation times larger than 15 min (yielding a layer thickness of about 300 nm) were not considered, but it is well known [27] that layers of several tens of microns can easily be obtained.

A less fortunate characteristic of the layers was that they displayed quite some macroscopic (i.e., on the scale of 10–100 μm) defects. When the peaks passed such a defect, the quality of the separations was completely deteriorated. We therefore had to be very careful in selecting a part of the channel devoid of such effects. Useful separation lengths longer than a few millimeter could not be obtained. Probably the defects are due to small fotoresit droplets which were not removed. To overcome this problem further investigation will be made on silicon wafers without channels (i.e. without pretreatment to produce the channels and to protect the channel walls against the HF enchant necessary to produce the porous layers). Another important problem encountered during the operation of the channels was that the quality of the layers deteriorated quite rapidly when their surface was cleaned to remove dust particles or adsorbed coumarin.

The porosity and the mean pore diameter are difficult to determine quantitatively from our SEM pictures. The use of more advanced porosity measurement techniques is difficult, since the amount of available porous material is far too small for the currently existing equipment. Krypton porisometry for example requires 3–4 g of porous material. From the SEM pictures we have estimated that the pore sizes vary between $d_{\text{pore}} = 5$ nm to 20 nm. These values however agree relatively well with those given in [22], showing that, for the same conditions as used in the present study (i.e., anodisation with a 15% HF solution), the typical pore diameter should lie between 10 and 20 nm. In [23], the pore size and the layer porosity were determined via TEM analysis. The porosity given in [23] for the presently considered range of conditions was 80–90%.

A more precise way to determine the layer porosity was pursued by comparing the fluorescence intensity I_{p} measured after injecting a given quantity of coumarin dyes in the porous SDC channels (prior to their derivatization with C_8) with that measured in a non-porous channel upon injection of the same sample amount. Assuming no light is emitted by the coumarin molecules occupying the pores of the porous

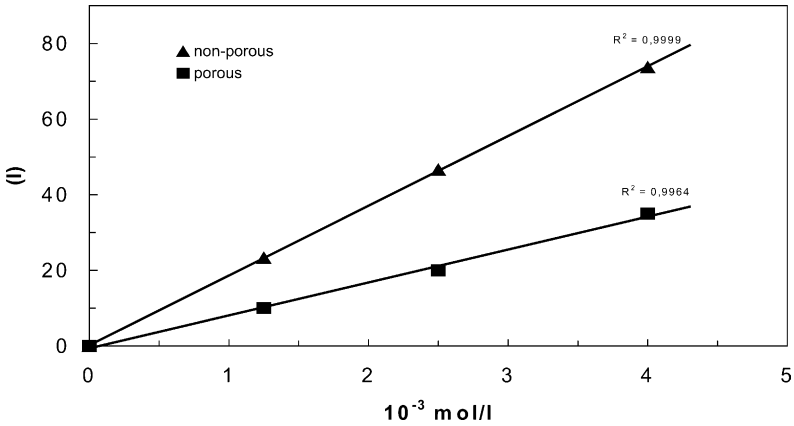

Fig. 3. Comparison of the fluorescence intensity measured after injecting a C450 sample at a given concentration in a 140 nm deep channel with and without a porous layer (porous layer depth = 200 nm).

silicon layer, the conservation of mass requires that:

$$I_{np} V_c = I_p (V_c + V_{pores}) \quad (3)$$

From Eq. (3), the total pore volume can be directly determined, which in turn allows to immediately determine the layer porosity from:

$$\varepsilon = \frac{V_{pores}}{V_c} \frac{d}{\delta} \quad (4)$$

In Fig. 3, the fluorescence intensities measured upon injection of three differently concentrated coumarin samples are shown. As can be noted, a nearly perfect linear relationship with the sample concentration is obtained for both the porous and the non-porous channels. Dividing the slopes of both regression lines, a value of 2.2 is obtained, which in turn yields a value of $V_{pores}/V_c = 1.2$. Using this value into Eq. (4) and using the ratio of the known channel and porous silicon layer depths (d = 140 and 200 nm respectively), a value of $\varepsilon = 0.84$ is obtained for the porous layer porosity. This value corresponds nicely to the values cited in [23] for similar anodisation conditions. According to the measurements in [22], the specific surface area in the large porosity range should be of the order of $a = 150 \times 10^6\ m^2/m^3$. Adopting this value, and considering that the increase (β) of the surface area available for coating is given by:

$$\beta = \frac{\text{total stationary phase surface area in porous layer}}{\text{bottom surface area of non} - \text{porous channel}} = \frac{a\delta A}{A} \quad (5)$$

it can easily be calculated that, with the given layer thickness of 200 nm, the application of the porous silicon layer has yielded a 30-fold increase of the stationary phase surface. Assuming that the pore wall surface can be coated at the same density of C_8 molecules as the channel bottom wall of the non-porous channels, this should also correspond to a 30-fold increase of the mass loadability, and hence [28] also to a 30-fold increase in detection sensitivity. With the present set-up, it was however not possible to fully substantiate this gain. Working with an on-column fluorescence imaging system, the molecules occupying the porous layer cannot significantly contribute to the detection signal. To demonstrate the gain in detection sensitivity, the detection should therefore occur at a position of the channel where the porous silicon layer is locally removed, and this will be the subject of a future study. Furthermore, given the fact that in the non-porous channel system used to obtain the I_{np} values shown in Fig. 3 we were already working at coumarin dye concentrations of the order of 5×10^{-3} M, i.e., already close to their dissolution limit, it was not possible to further increase the concentration of the injected samples.

Another important advantage of the application of the porous silicon layers should be the increase of the retention capacity of the channels. To quantify this increase, we have compared the zone retention factor k'' of one of our porous silicon channels with that of a non-porous SDC channel coated with a C_8 monolayer with the same depth. Individually injecting C440 and C450 samples in mobile phase flows with varying water methanol composition, the values for k'' were determined from the migration distance L_{eff} (cf. Eq. (1)) of the peak after a given flow time (t_{flow} = 1.5 s in all experiments). As can be noted from Fig. 4, the increase in retention capacity induced by the presence of the porous silicon layer is impressive. Whereas the mono-layer coated non-porous channel requires at least a 60% (v/v) water composition to induce any notable retention effect, the porous layer coated channel already displays retention factors of the order of $k'' = 3$ at a 10% (v/v) water composition. At a 50% (v/v) water composition, the C450 dye was already completely irreversibly retained at the inlet front of the porous silicon layer.

CCD camera images of two of the conducted separation experiments were made. In an overlay plot, the pixel intensity values obtained after vertically integrating the intensity signal over the inner 500 μm of the channel cross-section using the Simple PCI image analysis software are given. The C440 and C450 components can easily be base line separated

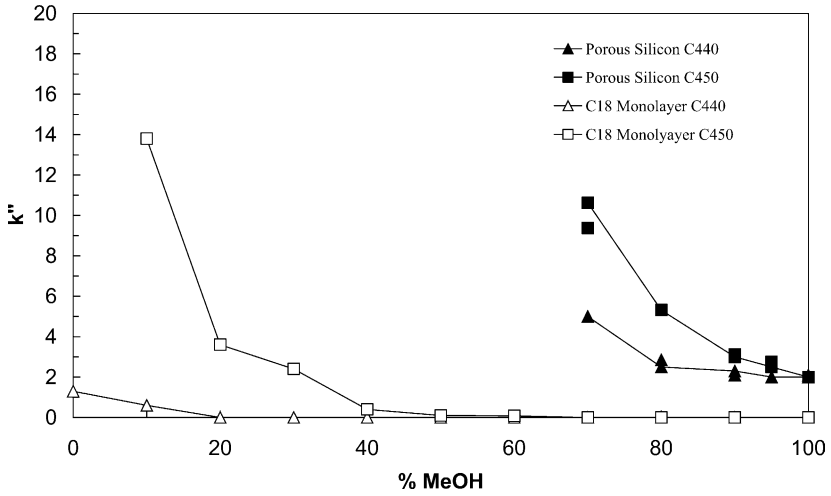

Fig. 4. Influence of the presence of the porous silicon layer on the zone retention factors for C440 and C450 as a function of the mobile phase composition (both channels had a flow-through depth of $d = 140$ nm, the porous layer had a depth of 200 nm). The different components were injected individually.

in the first millimeter of the channel. Injection of the individual components showed that the last retained peak was the C440 coumarin, in agreement with the reversed-phase capillary electrochromatography (CEC) measurements presented in [29].

The separation times (1.3 and 0.6 s at 2 and 4 mm/s flow velocity, respectively) are about an order of magnitude shorter than the separation time (about 20 s) in the on-chip open-tubular CEC system used in [29], is a direct consequence of the fact that the channel used in the present system is much thinner ($d + \delta = 340$ nm versus 2.9 and 4.7 μm in [29]) and, even more importantly, because the SDC concept allows to realize mobile phase velocities well in the cm/s-range, a range which is completely inaccessible in a typical CEC system.

A summary of the obtained H values is presented in Fig. 5. As can be noted, the presently considered SDC channel system yields sub-μm plate heights (as small as $H_{min} = 0.5$ μm) over a relatively broad range. In Fig. 5, the experimental plate heights are compared to the theoretically expected values calculated from the analytical plate height expression established in [3]:

$$H = 2\frac{D_m}{u}\left(1 + k''\frac{D_s}{D_m}\right) + \frac{2}{30}\frac{1 + 7k'' + 16k''^2}{(1 + k'')^2}u\frac{d^2}{D_m} + \frac{2}{3}\frac{k''}{(1 + k'')^2}u\frac{\delta^2}{D_s} \quad (6)$$

In Eq. (6), the stationary zone contribution to the diffusion term (D_s in first term of Eq. (6)) has been neglected, as we assume that the pores in the porous silicon layer are essentially running perpendicular to the channel bottom and are not sideways (i.e., in the axial direction) connected. In Eq. (6), all parameters are known, except for the molecular diffusivities. For the mobile phase diffusion coefficient, a value of $D_m = 510^{-10}$ m^2/s was used. For the porous layer, a number of different D_s values was considered. As can be noted from Fig. 5, the influence of the actual value of D_s is rather small in the explored range of mobile phase velocities. As can be noted, the experimental data points fit nicely to the theoretical predictions based on Eq. (6) and there is a relatively broad range (around $u = 3$–5 mm/s) wherein sub-μm plate heights are obtained.

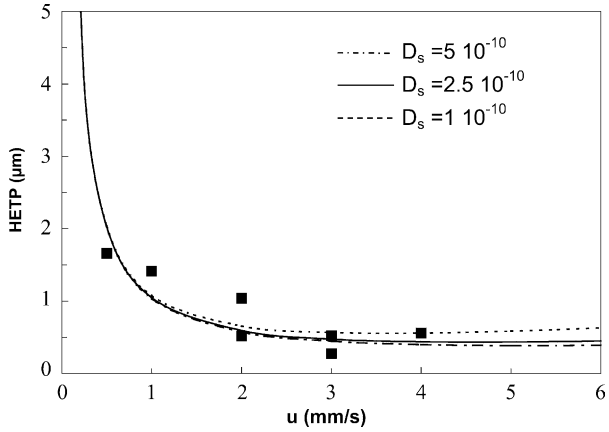

Fig. 5. van Deemter plot of the plate heights C450 peaks and comparison with the theoretically expected values obtained from Eq. (6) by putting $d = 140$ nm, $d = 200$ nm, $D_m = 5 \times 10^{-10}$ m^2/s and $k'' = 3$. The different lines correspond to different values of the (unknown) porous layer diffusion coefficient D_s.

4. Conclusions

Shear-driven chromatography channels with an integrated porous silicon layer have been successfully prepared and tested. The layers had a depth varying between 20 and 300 nm. Using these layers in combination with sub-μm thin flow-through channels, very large phase ratios, i.e., much larger than what is commonly the case in open-tubular LC and CEC systems, could be obtained. The porous

silicon layers had a very large internal porosity (order $\varepsilon = 0.85$) and allowed for the same type of derivatization procedures as for the silica based materials typically used in LC. The effect of the porous layer was clearly demonstrated by the strong increase in zone retention factor as compared to the reference mono-layer coated nano-channel system.

Owing to the nanometric channel thickness which could be allowed for by generating the flow according to the SDC principle, plate height values as small as $H = 0.5\,\mu m$ (retained component with $k'' = 3$) can be realized. This is in full agreement with the theoretical expectations and more than one order of magnitude smaller than what can be achieved in a packed-bed HPLC column with the same phase ratio ($V_s/V_m = 1.5$). The achieved separation times, order of 0.5–1 s, are also very small, even when compared to on-chip open-tubular CEC.

A number of practical problems however still need to be resolved (presence of peak disturbing defects in the layers, poor mechanical resistance to cleaning) before it will be possible to use the porous silicon layer coated SDC channels on a routine-like basis.

5. Nomenclature

a	specific internal surface area (m^{-1})
A	total channel bottom surface (m^2)
d	channel thickness (flowing zone only) (m).
D_m	molecular diffusion coefficient (m^2/s).
H	theoretical plate height (m)
I_{np}, I_p	fluorescence intensity, respectively in a non-porous and porous channel
k''	zone retention factor
L_0	distance traveled by unretained species peak (m), see Fig. 5a
L_{eff}	distance traveled by given retained species peak (m), see Fig. 5a
N	theoretical plate number
S_c	total coated pore wall surface area (m^2)
u	mean mobile phase velocity (m/s)
u_{wall}	velocity of moving wall (m/s)
V_c	volume of channel zone ($=Ad$) (m^3)
V_m	volume of mobile phase zone ($=Ad$) (m^3)
V_{pores}	total pore volume of porous silicon layer (m^3)
w	width of injected sample band (m)

Greek letters

β	ratio of stationary surface area in a porous and a non-porous SDC-channel (cf. Eq. (5))
δ	porous layer depth (m)
ε	porous layer porosity
σ_x^2	peak variance in space domain (m^2).

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